COURSE OBJECTIVES
You will learn the basic concepts, methods, and technologies needed to analyze, specify, design, build, and test combinational and synchronous sequential logic circuits with standard integrated circuits and programmable logic devices.

STUDENT LEARNING OUTCOMES – By the end of the course, you will have demonstrated an ability to do the following.

1. Apply knowledge of basic discrete mathematics and computer engineering principles.
2. Design small digital systems that meet a specified need within realistic constraints.
3. Use modern industry standard design tools.

INSTRUCTOR
Bill Carroll, Professor, Computer Science and Engineering
Office: ERB 521 Office Hours: MTuWTh 4:00 to 6:00 PM, or by appointment or chance.
Phone: 817-272-3787 Email: carroll@uta.edu
Course web-site: Blackboard, https://elearn.uta.edu
Faculty profile: https://www.uta.edu/profiles/bill-carroll

LABORATORY INSTRUCTOR
Rushi Dixit, Section 002. Office: ERB 127.
Office Hours: MTu 4:30 to 6:30 PM. Email: rushikeshdattat.dixit@mavs.uta.edu.
Rushi Dixit, Section 003. Office: ERB 127.
Office Hours: MTu 4:30 to 6:30 PM. Email: rushikeshdattat.dixit@mavs.uta.edu.

TIME AND PLACE
Section 001 (lecture) – TuTh 11:00 AM to 12:20 PM, ERB 131
Section 002 (lab) – Fr 2:00 to 4:50 PM, ERB 127
Section 003 (lab) – Fr 9:00 to 11:50 AM, ERB 127

PREREQUISITES – CSE 1320 and CSE 2315

TEXTBOOK – Manuscripts of selected chapters from Nelson, Carroll, Nagle, Irwin, Digital Logic Circuit Analysis & Design, 2nd, posted on Blackboard, https://elearn.uta.edu

HANDOUTS – posted on Blackboard, https://elearn.uta.edu

GRADING
A: 100-90, B: 89-80, C: 79-70, D: 69-60, F: 59-0 with points computed as follows.
0.20*Exam1 + 0.20*Exam2 + 0.20*FinalExam + 0.15*LabAverage + 0.15*DesignProject + 0.10*(HomeWorkAverage&ClassParticipation).

Students not completing one or more of these requirements may receive an Incomplete grade (I) in the course.

EXAMINATIONS
There will be two examinations during the semester plus a comprehensive final exam. See the lecture schedule for the dates. Examinations will be closed book and closed notes.
HOMEWORK

Homework will be given on a regular basis, will be graded, and will count toward your course grade both directly and indirectly. Late homework will generally not be accepted. Some assignments will involve Verilog programming, so you must have access to a computer that is capable of running the Quartus II 13.0sp1 (64-bit) Web-Edition CAD software. Download the software from here http://dl.altera.com/13.0sp1/?edition=web.

ACTIVE LEARNING

Active learning exercises will be performed in class on a regular basis to help you better understand the concepts being covered in the course. These exercises will typically be done in small groups. All students are expected to participate. Some may be graded and count as homework and class participation.

LABORATORY

Laboratory exercises and experiments are designed to reinforce materials presented in class and to give you experience in designing, building, and testing digital logic circuits. Please see the laboratory schedule for more details. Lab sessions meet in ERB 127.

TERM PROJECT (ABET project)

There will be an individual term design project toward the end of the course. The project will include design, implementation, testing and documentation of a small digital system to meet user specifications within realistic constraints. More details on the project will be provided later in the semester. This project must be completed and the project report submitted in order to receive a final grade (A,B,C,D,F) in the course. Those not submitting a final project report will get a grade of Incomplete or F depending upon their grade on other course work.

POLICIES

1. Academic Integrity – Students enrolled in all UT Arlington courses are expected to adhere to the UT Arlington Honor Code.

   I pledge, on my honor, to uphold UT Arlington’s tradition of academic integrity, a tradition that values hard work and honest effort in the pursuit of academic excellence.

   I promise that I will submit only work that I personally create or contribute to group collaborations, and I will appropriately reference any work from other sources. I will follow the highest standards of integrity and uphold the spirit of the Honor Code.

   UT Arlington faculty members may employ the Honor Code as they see fit in their courses, including (but not limited to) having students acknowledge the honor code as part of an examination or requiring students to incorporate the honor code into any work submitted. Per UT System Regents’ Rule 50101, §2.2, suspected violations of university’s standards for academic integrity (including the Honor Code) will be referred to the Office of Student Conduct. Violators will be disciplined in accordance with University policy, which may result in the student’s suspension or expulsion from the University. Additional information is available at https://www.uta.edu/conduct/.

2. Attendance – At The University of Texas at Arlington, taking attendance is not required but attendance is a critical indicator in student success. Each faculty member is free to develop his or her own methods of evaluating students’ academic performance, which includes establishing course-specific policies on attendance. However, while UT Arlington does not require instructors to take attendance in their courses, the U.S. Department of Education requires that the University have a mechanism in place to mark when Federal Student Aid recipients “begin attendance in a course.” UT Arlington instructors will report when students begin attendance in a course as part of the final grading process. Specifically, when assigning a student a grade of F, faculty report the last date a student attended their class based on evidence such as a test, participation in a class project or presentation, or an engagement online via Blackboard. This date is reported to the Department of Education for federal financial aid recipients. My policy for this course – You are expected to attend class and attendance will be checked on a regular basis. Those with more than three unexcused absences from the lecture and/or laboratory will have their final average reduced by five points for each additional absence before their final letter grade is assigned.
3. **Campus Carry** – Effective August 1, 2016, the Campus Carry law (Senate Bill 11) allows those licensed individuals to carry a concealed handgun in buildings on public university campuses, except in locations the University establishes as prohibited. Under the new law, openly carrying handguns is not allowed on college campuses. For more information, visit [http://www.uta.edu/news/info/campus-carry/](http://www.uta.edu/news/info/campus-carry/)

4. **Cell phones and wireless devices** – Please refrain from using cell phones during class times. All electronic devices must be powered off during examinations. Use of tablets or laptops for viewing class materials is permitted.

5. **Disability Accommodations** – UT Arlington is on record as being committed to both the spirit and letter of all federal equal opportunity legislation, including The Americans with Disabilities Act (ADA), The Americans with Disabilities Amendments Act (ADAAA), and Section 504 of the Rehabilitation Act. All instructors at UT Arlington are required by law to provide “reasonable accommodations” to students with disabilities, so as not to discriminate on the basis of disability. Students are responsible for providing the instructor with official notification in the form of a letter certified by the Office for Students with Disabilities (OSD). Only those students who have officially documented a need for an accommodation will have their request honored. Students experiencing a range of conditions (Physical, Learning, Chronic Health, Mental Health, and Sensory) that may cause diminished academic performance or other barriers to learning may seek services and/or accommodations by contacting:
   - **The Office for Students with Disabilities, (OSD)** [www.uta.edu/disability](http://www.uta.edu/disability) or calling 817-272-3364.
   - **Counseling and Psychological Services, (CAPS)** [www.uta.edu/caps/](http://www.uta.edu/caps/) or calling 817-272-3671.

6. **Drop Policy** – Students may drop or swap (adding and dropping a class concurrently) classes through self-service in MyMav from the beginning of the registration period through the late registration period. After the late registration period, students must see their academic advisor to drop a class or withdraw. Undeclared students must see an advisor in the University Advising Center. Drops can continue through a point two-thirds of the way through the term or session. It is the student’s responsibility to officially withdraw if they do not plan to attend after registering. **Students will not be automatically dropped for non-attendance**. Repayment of certain types of financial aid administered through the University may be required as the result of dropping classes or withdrawing. For more information, contact the Office of Financial Aid and Scholarships ([http://wweb.uta.edu/aao/fao/](http://wweb.uta.edu/aao/fao/)).

7. **Electronic communication** – UT Arlington has adopted MavMail as its official means to communicate with students about important deadlines and events, as well as to transact university-related business regarding financial aid, tuition, grades, graduation, etc. All students are assigned a MavMail account and are responsible for checking the inbox regularly. There is no additional charge to students for using this account, which remains active even after graduation. Information about activating and using MavMail is available at [http://www.uta.edu/oit/cs/email/mavmail.php](http://www.uta.edu/oit/cs/email/mavmail.php).

8. **Emergency Exit Procedures** – Should we experience an emergency event that requires us to vacate the building, students should exit the room and move toward the nearest exit, which is located down the hallway to the left as you exit ERB 131 and straight ahead as you exit ERB 127. When exiting the building during an emergency, one should never take an elevator but should use the stairwells. Faculty members and instructional staff will assist students in selecting the safest route for evacuation arrangements and will make to assist individuals with disabilities.

9. **Final Review Week** – For semester-long courses, a period of five class days prior to the first day of final examinations in the long sessions shall be designated as Final Review Week. The purpose of this week is to allow students sufficient time to prepare for final examinations. During this week, there shall be no scheduled activities such as required field trips or performances; and no instructor shall assign any themes, research problems or exercises of similar scope that have a completion date during or following this week **unless specified in the class syllabus**. During Final Review Week, an instructor shall not give any examinations constituting 10% or more of the final grade, except makeup tests and laboratory examinations. In addition, no instructor shall give any portion of the final examination during Final Review Week. During this week, classes are held as scheduled. In addition, instructors are not required to limit content to topics that have been previously covered; they may introduce new concepts as appropriate.

10. **Grade appeals** – Should you have a concern about the grade you received on an assignment or exam, you may submit a re-grading request to the instructor or TA in writing within two class days from the day the assignment or exam was returned. Appeal of the final course grade should follow the established UT Arlington policy which begins with a written appeal to the course instructor of record. You can learn more about grade appeals and other academic regulations at [http://wwwb.uta.edu/catalog/content/general/academic_regulations.aspx#17](http://wwwb.uta.edu/catalog/content/general/academic_regulations.aspx#17).

11. **Make-up work** – Late homework will not be accepted and cannot be made up. Make up of missed examinations and laboratory assignments will be handled case-by-case and, generally, be approved only if sufficient justification can be
made and documented. Requests for make-up must be made to the instructor within one week of the missed work’s due date.

12. **Non-Discrimination Policy** – The University of Texas at Arlington does not discriminate on the basis of race, color, national origin, religion, age, gender, sexual orientation, disabilities, genetic information, and/or veteran status in its educational programs or activities it operates. For more information, visit [uta.edu/eos](http://uta.edu/eos).

13. **Preparation for class** – You are expected to read the appropriate sections of the textbook and supplemental material prior to each class and/or lab session.

14. **Student Feedback Survey** – At the end of each term, students enrolled in face-to-face and online classes categorized as “lecture,” “seminar,” or “laboratory” are directed to complete an online Student Feedback Survey (SFS). Instructions on how to access the SFS for this course will be sent directly to each student through MavMail approximately 10 days before the end of the term. Each student’s feedback via the SFS database is aggregated with that of other students enrolled in the course. Students’ anonymity will be protected to the extent that the law allows. UT Arlington’s effort to solicit, gather, tabulate, and publish student feedback is required by state law and aggregate results are posted online. Data from SFS is also used for faculty and program evaluations. For more information, visit [http://www.uta.edu/sfs](http://www.uta.edu/sfs).

15. **Student Support Services** – UT Arlington provides a variety of resources and programs designed to help students develop academic skills, deal with personal situations, and better understand concepts and information related to their courses. Resources include tutoring, major-based learning centers, developmental education, advising and mentoring, personal counseling, and federally funded programs. For individualized referrals, students may visit the reception desk at University College (Ransom Hall), call the Maverick Resource Hotline at 817-272-6107, send a message to resources@uta.edu, or view the information at [http://www.uta.edu/universitycollege/resources/index.php](http://www.uta.edu/universitycollege/resources/index.php). Engineering Student Services, 242 Nedderman Hall, is another resource for guidance on academic and career questions.

16. **Title IX** – The University of Texas at Arlington ("University") is committed to maintaining a learning and working environment that is free from discrimination based on sex in accordance with Title IX of the Higher Education Amendments of 1972 (Title IX), which prohibits discrimination on the basis of sex in educational programs or activities; Title VII of the Civil Rights Act of 1964 (Title VII), which prohibits sex discrimination in employment; and the Campus Sexual Violence Elimination Act (SaVE Act). Sexual misconduct is a form of sex discrimination and will not be tolerated. For information regarding Title IX, visit [www.uta.edu/titleIX](http://www.uta.edu/titleIX) or contact Ms. Jean Hood, Vice President and Title IX Coordinator at (817) 272-7091 or jmhoo@uta.edu.
<table>
<thead>
<tr>
<th>Week</th>
<th>Weekly Reading</th>
<th>Class date</th>
<th>Tuesday (1) Lecture Topics</th>
<th>Class date</th>
<th>Thursday (2) Lecture Topics</th>
<th>Lab date</th>
<th>Lab topics</th>
<th>HW Due Dates</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.0-0.7</td>
<td>1/16</td>
<td>Course overview, digital systems, basic gates: AND, OR, NOT, NAND, NOR, XOR, basic adders. Lab 0 preview.</td>
<td>1/18</td>
<td>Combinational circuits; truth tables, functions, logic equations; number systems.</td>
<td>1/19</td>
<td>Lab 0 -- Lab resources, policies and procedures, DE1, BitBoard, basic logic gates. [BB]</td>
<td>HW#1 -- 1/23</td>
</tr>
<tr>
<td>2</td>
<td>1.0-1.3, 2.0-2.2</td>
<td>1/23</td>
<td>Signed-number representation, two's complement number systems and arithmetic. Digital codes. Lab 1 preview.</td>
<td>1/25</td>
<td>Boolean algebra -- postulates and theorems. Functions and equations -- minterms, maxterms, SOP, POS, canonical forms.</td>
<td>1/26</td>
<td>Lab 1 -- Introduction to Quartus II.</td>
<td>HW#2 -- 1/30</td>
</tr>
<tr>
<td>3</td>
<td>1.4-1.6, 2.3-2.4</td>
<td>1/30</td>
<td>Minimization of logic equations and combinational circuits. Minimal forms. Lab 2 preview.</td>
<td>2/1</td>
<td>Karnaugh maps. Incompletely specified functions.</td>
<td>2/2</td>
<td>Lab 2 -- Basic Adders. Two's-complement adder/subtractor. [BB]</td>
<td>HW#3 -- 2/6</td>
</tr>
<tr>
<td>4</td>
<td>2.5.</td>
<td>2/6</td>
<td>Combinational logic circuit design and analysis. Timing diagrams.</td>
<td>2/8</td>
<td>Combinational logic circuit analysis. Propagation delay.</td>
<td>2/9</td>
<td>Catch-up or get-ahead week.</td>
<td>HW#4 -- 2/13</td>
</tr>
<tr>
<td>5</td>
<td>3.0-3.2, 3.4-3.5</td>
<td>2/13</td>
<td>Catch up, design examples, and review. Lab 3 preview.</td>
<td>2/15</td>
<td>Examination 1.</td>
<td>2/16</td>
<td>Lab 3 -- DE1 programming and I/O. [DE1]</td>
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<tr>
<td>6</td>
<td></td>
<td>2/20</td>
<td>Verilog modeling and programming. Lab 4 preview.</td>
<td>2/22</td>
<td>Higher-level combinational logic. Return exam 1.</td>
<td>2/23</td>
<td>Lab 4 -- Seven-segment displays and decoders. [DE1]</td>
<td>HW#5 -- 2/27</td>
</tr>
<tr>
<td>7</td>
<td>3.3.</td>
<td>2/27</td>
<td>Sequential circuits, flip-flops, registers, and counters. Lab 5 preview.</td>
<td>3/1</td>
<td>Verilog modeling of synchronous circuits. Circuit analysis.</td>
<td>3/2</td>
<td>Lab 5 -- Four-function arithmetic/logic unit (ALU). [DE1]</td>
<td>HW#6 -- 3/8</td>
</tr>
<tr>
<td>8</td>
<td>4.0-4.6.</td>
<td>3/6</td>
<td>Synchronous circuit design. Lab 6 preview.</td>
<td>3/8</td>
<td>Design examples -- controllers.</td>
<td>3/9</td>
<td>Catch-up or get-ahead week.</td>
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<tr>
<td>9</td>
<td>5.0-5.2.</td>
<td>3/13</td>
<td>Spring Break</td>
<td>3/15</td>
<td>Spring Break</td>
<td>3/16</td>
<td>Spring Break</td>
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</tr>
<tr>
<td>11</td>
<td>5.4-5.5.</td>
<td>3/27</td>
<td>Catch up, design examples, and review. Lab 7 preview.</td>
<td>3/29</td>
<td>Examination 2.</td>
<td>3/30</td>
<td>Lab 7 -- FSMs and controllers. [BB]</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>4/10</td>
<td>4/12</td>
<td>Programmable logic. FPGAs. Cyclone II. Lab 9 preview.</td>
<td>4/13</td>
<td>Design examples.</td>
<td>4/24</td>
<td>Design project. [DE1]</td>
<td>HW#9 -- 4/24</td>
</tr>
<tr>
<td>14</td>
<td>5.3.</td>
<td>4/24</td>
<td>Timers and clocks.</td>
<td>4/26</td>
<td>Design examples.</td>
<td>4/27</td>
<td>Design project. [DE1]</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>5/1</td>
<td>5/3</td>
<td>Design examples.</td>
<td>5/4</td>
<td>Review.</td>
<td>5/5</td>
<td>Project demo deadline -- 5:00 PM. Report deadline -- 11:59 PM.</td>
<td></td>
</tr>
</tbody>
</table>

5/8 Final exam -- 11:00 AM to 1:30 PM